What is claimed is:

1. A process for manufacturing an integrated circuit, the process comprising:

providing a substrate comprising a dielectric layer (e.g., 1) over a conductive material (e.g., 3, 5);

depositing a hardmask (e.g., 7) over the dielectric layer (e.g., 1);

applying a first photoresist (e.g., 9) over the hardmask (e.g., 7) and photodefining at least one first elongated opening (e.g., 11);

etching the hardmask (e.g., 7) and partially etching the dielectric (e.g., 1) to deepen the at least one first elongated opening to form a trench (e.g., 13), the trench having a bottom in the dielectric layer (e.g., 1);

removing the first photoresist (e.g., 9);

applying a second photoresist (e.g., 15) and photodefining at least one second elongated opening (e.g., 17, 19) across the at least one trench (e.g., 13);

etching the exposed dielectric (e.g., 1) from the bottom of the at least one trench (e.g., 13) down to the underlying conductive material (e.g., 3.5).

2. The process of claim 1, further comprising removing the second photoresist (e.g., 15).

3. The process of claim 1, further comprising removing the hardmask (e.g. 7).

4. The process of claim 1, further comprising metallization and planarization.

5. The process of claim 1, wherein the dielectric layer (e.g., 1) is silicon dioxide.

6. The process of claim 1, wherein the hardmask (e.g., 7) is silicon nitride.

7. The process of claim 1, wherein the step of etching the exposed dielectric (e.g., 1) from the bottom of the at least one trench (e.g., 13) down to the underlying conductive material (e.g., 3, 5) forms at least one third opening (e.g., 18, 20) to

the underlying conductive material (e.g., 3, 5) and the at least one third opening (e.g., 18, 20) is filled with conductive material to form a contact or a via (e.g., 23, 25).

8. The process of claim 1, wherein the step of etching the exposed dielectric (e.g., 1) forms at least one third opening (e.g., 18, 20) that has substantially a quadrilateral cross-section.

9. The process of claim 1, wherein the step of etching the exposed dielectric (e.g., 1) forms at least one third opening (e.g., 18, 20) that has substantially a square cross-section.

10. The process of claim 1, wherein the step of etching the exposed dielectric (e.g., 1) forms at least one third opening (e.g., 18, 20) that has substantially a rectangular cross-section.

11. The process of claim 1, wherein the step of etching the exposed dielectric (e.g., 1) forms at least one third opening (e.g., 18, 20) that has a feature size of about 0.5 micron or less.

12. The process of claim 1, wherein substantially no etch stop layer is deposited at the bottom of the trench.

13. A process for manufacturing an integrated circuit, the process comprising:

providing a substrate comprising silicon dioxide dielectric layer (e.g., 1) over a conductive material;

depositing a silicon nitride hardmask (e.g., 7) over the dielectric layer;

applying a first photoresist (e.g., 9) over the hardmask and photodefining at least one elongated opening;

etching the hardmask and partially etching the dielectric to deepen the at least one elongated opening (e.g., 11) to form at least one trench (e.g., 13), the trench forming a bottom in the dielectric layer (e.g., 1);

stripping the first photoresist (e.g., 9);

applying a second photoresist (e.g., 15) and photodefining at least one second elongated opening (e.g., 17, 19) across the at least one trench;

selectively etching the dielectric (e.g., 1) from the bottom of the trench (e.g., 13) down to the underlying conductive material (e.g., 3, 5); and

removing the second photoresist (e.g., 15) and the hardmask (e.g., 7).

14. A method of making an integrated circuit comprising defining a via or contact (e.g., 23, 25) by the intersection of a first elongated opening (e.g., 11) in a first mask (e.g., 9) and a second (e.g., 17, 19) elongated opening in a second mask (e.g., 15) , and using at least one of the mask openings to define the location of a conductor (e.g., 3, 5) to which the via or contact (e.g., 23, 25) is to be connected.

15. An integrated circuit, comprising at least one connection (e.g., 23, 25), wherein the at least one connection has substantially a quadrilateral cross-section, wherein the quadrilateral has a feature size of about 0.5 micron or less.

16. The integrated circuit of claim 15, further comprising at least one trench having a bottom (e.g., 13), wherein there is substantially no etch stop layer at the bottom of the trench.

17. The integrated circuit of claim 15, wherein the at least one connection (e.g., 23, 25) has substantially a square cross-section.

18. The integrated circuit of claim 15, wherein the at least one connection (e.g., 23, 25) has substantially a rectangular cross-section.

19. The integrated circuit of claim 15, wherein the at least one connection (e.g., 23, 25) is a contact or a via.

20. The integrated circuit of claim 15, wherein the quadrilateral has a feature size of about 0.25 micron or less.

21. An integrated circuit, comprising at least one connection (e.g., 23, 25), wherein the at least one connection has substantially a quadrilateral cross-section, wherein the quadrilateral has a feature size of about 0.18 to about 0.14 micron.

22. The integrated circuit of claim 21, wherein the quadrilateral has a feature size of about 0.18 to about 0.16 micron.

23. An integrated circuit, comprising a connection, wherein the connection (e.g., 23, 25) has substantially a quadrilateral cross-section, wherein the quadrilateral has a feature size of about 0.12 micron.